Amendments to the Claims

This listing of claim will replace all prior versions and listings of claim in the application.

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1. (currently amended) An improved capacitive sensing circuit comprising:

a sense pulse generator having an output , said output having ~~providing~~ a first polarity sense pulse during a first phase and a second polarity sense pulse during a second phase;

a sense capacitor coupled to the sense pulse generator;

a detector coupled to the sense capacitor; and

a storage device coupled to the detector.

2. (original) The circuit of claim 1 wherein the storage device is a sample and hold circuit.

3. (original) The circuit of claim 2 wherein the sample and hold circuit further comprises an amplifier and a capacitor.

4. (original) The circuit of claim 1 wherein the storage device comprises a capacitor.

5. (original) The circuit of claim 1 further including a filter coupled to the storage device.

6. (cancelled)

7. (currently amended) The circuit of claim [6] 1 further including a demodulation circuit coupled to the storage device.

8. (original) The circuit of claim 7 wherein said demodulation circuit comprises a filter having an input and an output, and a nonlinear element having a first input, wherein said nonlinear element is selected from one of the following: a switch, a multiplier, a mixer.

9. (original) The circuit of claim 8 wherein said filter includes a high-pass characteristic and said filter output is coupled to said first input of the nonlinear element.

10. (original) The circuit of claim 8 wherein said filter includes a low-pass characteristic, said nonlinear element includes an output, and said filter input is coupled to said output of the nonlinear element.

11. (original) The circuit of claim 8 wherein said nonlinear element further includes a second input coupled to a signal synchronous with sense pulse polarity.

12. (original) The circuit of claim 8 wherein said demodulation circuit further comprises an input and an output, and an analog signal is provided to said demodulation circuit input.

13. (original) The circuit of claim 8 wherein said demodulation circuit further comprises an input and an output, and a digital signal is provided to said demodulation circuit input.

14. (original) The circuit of claim 1 further including a second sense capacitor coupled to the detector and the sense pulse generator.

15. (original) The circuit of claim 14 further including a third and a fourth capacitor coupled to the detector and the sense pulse generator, wherein said sense pulse generator generates a first set of sense pulses on the first through fourth sense capacitors and a second set of sense pulses on the first through fourth sense capacitors.

16. (original) The circuit of claim 15 wherein the first, second, third and fourth capacitors form a portion of a microstructure, and said detector comprises an output, said output being responsive to the orientation of said microstucture.

17. (original) The circuit of claim 1 further including an analog to digital converter coupled to the storage device.

18. (original) The circuit of claim 17 further including a demodulator coupled to the output of the analog to digital converter.

19. (original) The circuit of claim 1 wherein said first sense pulse comprises a voltage pulse, and said second sense pulse comprises a voltage pulse.

20. (original) The circuit of claim 1 wherein said first sense pulse comprises a charge pulse, and said second sense pulse comprises a charge pulse.

21. (original) The circuit of claim 1 wherein said detector comprises a charge detector.

22. (original) The circuit of claim 1 wherein said detector comprises a voltage detector.

23-35. (withdrawn)

36. (currently amended) A circuit, comprising:

a sense capacitor coupled to a microstructure;

a charge detector coupled to the sense capacitor;

a sense pulse generator coupled to said sense capacitor and having an output, said sense pulse generator comprising control circuitry, said control circuitry causing the sense pulse polarity at the output to invert over two phases; and

sense circuitry coupled to the charge detector detecting the difference between the phases.

37. (original) The circuit of claim 36 wherein the charge detector comprises a buffer amplifier.

38. (original) The circuit of claim 36 wherein the charge detector comprises a charge integrator.

39. (original) The circuit of claim 36 wherein the sense circuitry comprises:

a storage device coupled to the charge detector;

a demodulator coupled to the storage device.

40. (original) The circuit of claim 36 further including:

a storage device coupled to the charge detector;

an analog-to-digital converter coupled to the output of the storage device; and

a digital demodulator coupled to the analog-to-digital converter.

A2 (cont.)

41-44. (withdrawn)

45. (currently amended) A method of operating a switched-capacitor circuit, comprising:

providing a plurality of sense pulses from the output of a sense pulse generator having a first polarity to a sense capacitor during a first phase to obtain a first output of the sense transducer; and

providing a plurality of sense pulses from the output of a sense pulse generator having a second polarity to a sense capacitor during a second phase to obtain a second output of the sense transducer.

46. (original) The method of claim 45 further including the step of storing the output of the sense capacitor.

47. (original) The method of claim 45 further including the step of sampling an output of the sense capacitor.

48. (original) The method of claim 47 further including demodulating the output of the first and the second phases.

49. (currently amended) An improved capacitive sensing circuit comprising:

a sense pulse generator having an output, the output providing a first magnitude sense pulse of a first polarity and a second magnitude sense pulse of a second polarity;

a sense capacitor coupled to the sense pulse generator;

a charge detector coupled to the sense capacitor;

a storage device coupled to the charge detector; and

a demodulator coupled to the storage device.